LCD MODULE
SPECIFICATION

Customer: _____

Model Name: HC070IK65057-E13

Date: 2021.04.27

Version: 01

■ **Preliminary Specification**

□ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

Record of Revision

Version	Revise Date	Page	Content
Pre-Spec.01	2021.04.27	All	Initial Release

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1.0 General description

1.1 Introduction

HC070IK65057-E13 **is model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 7.0(16:9) inch diagonally measured active display area with WSVGA (1024horizontal by 600 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.**

1.2 Features

- **TTL Interface**
- Data enable signal mode
- 24-bit color depth,display 16.7M colors
- Low driving voltage and low power consumption
- ROHS Compliant

1.3 General information

Item	Specification	Unit	Remarks
Outline Dimension	164.90(H) x 100.00(V) x5.61(body)	mm	
Display area	154.21(W) x85.92(H)	mm	
Number of Pixel	1024(H) x 600(V)	pixels	
Pixel pitch	0.1506(H) x 0.1432(V)	mm	
Pixel arrangement	Pixels RGB stripe arrangement		
Display mode	Normally Black		
Surface treatment	IPS Film		
Weight	TBD (Typ.)	gram	
Back-light	Single LED (Side-Light type)		

1.4 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	164.60	164.90	165.20	mm
	Vertical(V)	99.70	100.00	100.30	mm
	Depth(D)	5.41	5.61	5.81	mm

1.5 Backlight

Item	Symbol	Typ	MIN.	TYP.	MAX.	Unit	Note
Forward voltage	Vf	9.0	8.5	9.0	9.9	V	(1)(2)
Forward current	If	220	--	--	--	mA	(1)(2) (3)
Power Consumption	PBL	--	--	--	--	mW	

Note:

(1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Ta =25±2℃

(3) Test Condition: LED current 220 mA

2.0 OPTICAL CHARACTERISTICS

Item	Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle range	Horizontal	θ	CR > 10	80	85	--	Deg	
	Vertical	θ		80	85	--	Deg	
Contrast ratio		CR	θ = 0°	600：1	800：1	--	--	
Luminance		YL		600	650	--	Cd/cm2	
Transmittance		T(%)	θ = 0°	--	5.0	--	%	
Color Gamut (C light)				45	50	--	%	
White chromaticity		Xw	Θ=0°	TYP. -0.03	0.323	TYP. +0.03		
		Yw			0.333			
Reproduction of color （C-light）	Red	Rx			0.618			
		Ry			0.326			
	Green	Gx			0.285			
		Gy			0.539			
	Blue	Bx			0.146			
		By			0.148			
Response Time (Rising + Falling)	Trt		Ta= 25°C θ = 0°	--	25	40	ms	

3.0 INTERFACE PIN CONNECTION

3.1 Signal of interface

Terminal No.	Symbol	IO	Functions
1--2	VLED+	P	Power for LED backlight (Anode)
3--4	VLED-	P	Power for LED backlight (Cathode)
5	GND	P	Analog Ground
6	VCOM	I	Common voltage
7	DVDD	P	Power for Digital Circuit
8	MODE	I	DE/SYNC mode select
9	DE	I	Data Input Enable
10	VS	I	Vertical Sync Input
11	HS	I	Horizontal Sync Input
12	B7	I	Blue data(MSB)
13	B6	I	Blue data
14	B5	I	Blue data
15	B4	I	Blue data
16	B3	I	Blue data
17	B2	I	Blue data
18	B1	I	Blue data
19	B0	I	Blue data(LSB)
20	G7	I	Green data(MSB)
21	G6	I	Green data
22	G5	I	Green data
23	G4	I	Green data
24	G3	I	Green data
25	G2	I	Green data
26	G1	I	Green data
27	G0	I	Green data (LSB)
28	R7	I	Red data(MSB)
29	R6	I	Red data
30	R5	I	Red data
31	R4	I	Red data
32	R3	I	Red data
33	R2	I	Red data
34	R1	I	Red data
35	R0	I	Red data(LSB)
36	GND	P	Power Ground
37	DCLK	I	Sample clock
38	GND	P	Power Ground
39	L/R	I	Left / right selection
40	U/D	I	Up/down selection
41	VGH	P	Gate ON Voltage
42	VGL	P	Gate OFF Voltage
43	AVDD	P	Power for Analog Circuit
44	RESET	I	Global reset pin.

45	**NC**	**-**	**No connection**
46	**VCOM**	**I**	**Common Voltage**
47	**DITHB**	**I**	**Dithering function**
48	**GND**	**P**	**Power Ground**
49	**NC**	**-**	**No connection**
50	**NC**	**-**	**No connection**

4.0 Power On/Off Sequence

To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power on: VDD, GND → AVDD, AGND → V1 to V14
Power off: V1 to V14 → AVDD, AGND→ VDD, GND

4.1 Power on/off control

HX8282-A01 has a power on/off sequence control function. In order to prevent IC from power on reset fail, the rising time **(T_{POR})** of the digital power supply VDD should be maintained within the given specifications. Please refer to "AC Characteristics" for more detail on timing.

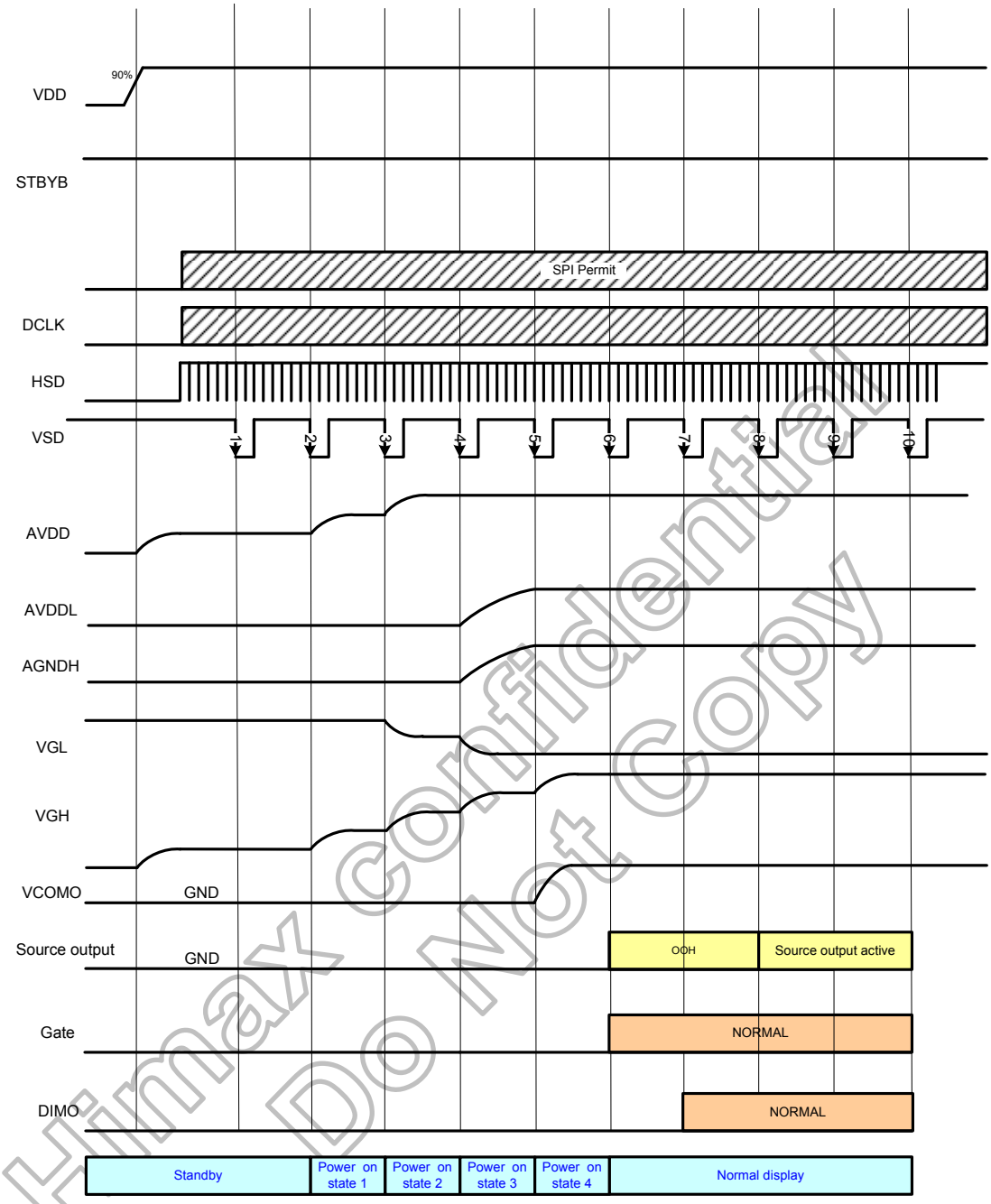
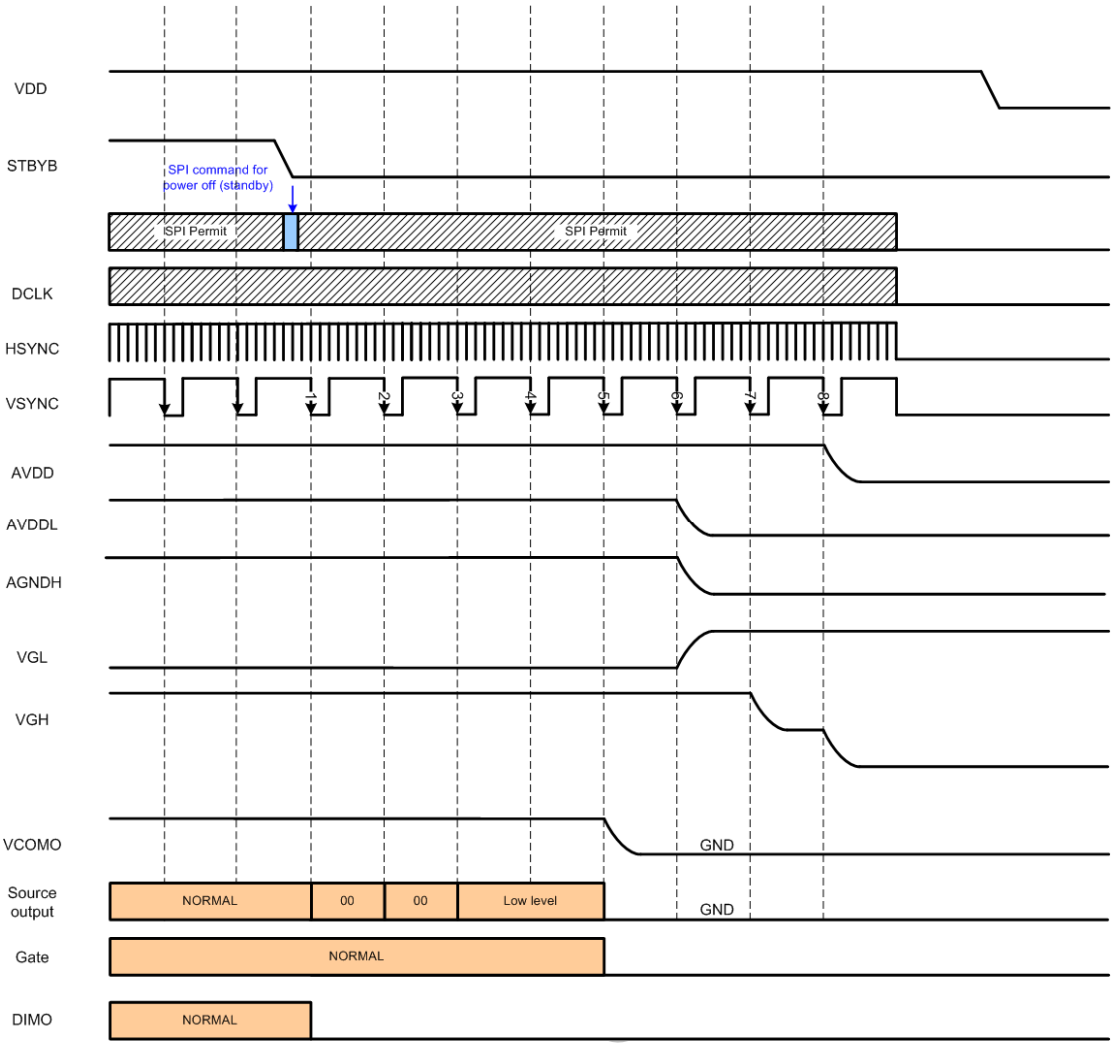


Figure: Power on timing sequence



Note: (1) Low level=3FH, when NBW=L. **(Normally white)**
(2) Low level=00H, when NBW=H. **(Normally black)**

Figure: Power off timing sequence

5.0 ELECTRICAL CHARACTERISTICS

5.1 TFT LCD Module

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	3.0	3.3	3.6	V
	VGH	17	18	19	V
	VGL	-7.0	-6.0	-5.0	V
	AVDD	9.4	9.6	10.2	V
VCOM	VCOM	3.1	(3.3)	3.6	V

Note:

(1) VGH is TFT Gate operating voltage.

(2) VGL is TFT Gate operating voltage. The low voltage level of VGH signal must be fluctuates with same phase as Vcom.

5.2 Back-Light Unit

The backlight system is an edge-lighting type with 33LED.

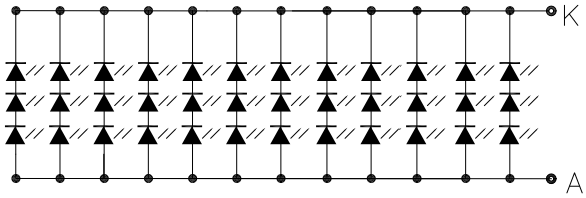
The characteristics of the LED are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	IL	-	220	-	mA	(2)
LED Voltage	VL	-	9.0	-	V	
Operating LED life time	Hr	20000	-	-	Hour	(1)(2)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ° C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=220mA. The LED lifetime could be decreased if operating IL is larger than 220mA. The constant current driving method is suggested.

LED CIRCUIT DIAGRAM： 3 x11= 33 LED



5.3 DC Characteristics

5.3.1 Absolute Maximum Rating (GND=AGND=0V)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	Vdd	-0.5	-	+3.96	V
Power supply voltage 2	Avdd	-0.5	-	+14.85	V
Logic Output voltage	Vout	-0.5	-	+5.0	V
Input voltage	Vin	-0.5	-	AVDD+0.5	V
Operation temperature	TOPR	-20	-	+70	℃
Storage temperature	TSTG	-30	-	+80	℃

Note: (1) All of the Voltages listed above are with respective to GND=0V.
(2) Device is subject to be damaged permanently if stresses belong those absolute maximum ratings listed above.

5.4 TTL mode DC electrical characteristics

(VDD=2.3 to 3.6V, AVDD=6.5 to 13.5V, GND=AGND=0V, T_A=-20℃ to +85℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Power supply voltage	VDD	-	2.3	-	3.6	V
Power supply voltage	AVDD	-	6.5	-	13.5	V
Power supply voltage	AVDDL	Full range application	6.5	-	13.5	V
		Half AVDD application	-	V8+0.1	-	V
Power supply voltage	AGNDH	Full range application		0		V
		Half AVDD application	-	V7-0.1	-	V
Low level input voltage	V_{IL}	For digital circuit	0	-	0.3VDD	V
High level input voltage	V_{IH}	For digital circuit	0.7VDD	-	VDD	V
Output low voltage	V_{OL}	I_{OL}=400μA	-	-	GND+0.4	V
Output high voltage	V_{OH}	I_{OH}=-400μA	VDD-0.4	-	-	V
Pull low/high resistance	R_i	For the digital input pin @VDD=3.3V	200	250	300	KΩ
Input leakage current	Ii	For digital circuit	-	-	±1	μA
Digital operation current	Idd	Fclk=50MHz, LD=48KHz,VDD=3.3V, No load	-	12	20	mA
Digital stand-by current	Ist1	Clock & all functions are stopped	-	10	50	μA
Analog operating current	Idda	No load, Fclk=50MHz,LD=48KHz @ AVDD=10V, V1=8V, V14=0.4V	-	8	10	mA
Analog stand-by current	Ist2	No load, clock & all functions are stopped	-	10	50	μA
Input level of V1~V7	Vref1	Gamma correction voltage input	0.4AVDD	-	AVDD-0.1	V
Input level of V8~V14	Vref2	Gamma correction voltage input	0.1	-	0.6AVDD	V
Output voltage deviation	Vod1	Vo=AGND+0.1V~AGND+0.5V & Vo=AVDD-0.5V~AVDD-0.1V	-	±20	±35	mV
Output voltage deviation	Vod2	Vo=AGND+0.5V~AVDD-0.5V	-	±15	±20	mV
Output voltage offset between chips	Voc	Vo=AGND+0.5V~AVDD-0.5V	-	-	±20	mV
Dynamic range of output	Vdr	SO1~SO1200	0.1	-	AVDD-0.1	V
Sinking current of outputs	IOLy	SO1~SO1200; Vo=0.1V vs. 1.0V, AVDD=13.5V	80	-	-	μA
Driving current of outputs	IOHy	SO1~SO1200 ;Vo=0.1V vs. 12.5V, AVDD=13.5V	80	-	-	μA
Resistance of gamma table	Rg	Rn: Internal gamma resistor	0.7xRn	1.0xRn	1.3xRn	Ω

Table : DC electrical characteristics

5.5 AC Characteristics

5.5.1 TTL mode AC electrical characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
VDD power on slew rate	T_{POR}	From 0V to 90% VDD	-	-	20	ms
GRB pulse width	T_{GRB}	-	50	-	-	μs
DCLK cycle time	T_{cph}	-	14	-	-	ns
DCLK pulse duty	T_{cwh}	-	40	50	60	%
VSD setup time	T_{vst}	-	5	-	-	ns
VSD hold time	T_{vhd}	-	5	-	-	ns
HSD setup time	T_{hst}	-	5	-	-	ns
HSD hold time	T_{hhd}	-	5	-	-	ns
Data setup time	T_{dsu}	D0[7:0], D1[7:0], D2[7:0] to DCLK	5	-	-	ns
Data hold time	T_{dhd}	D0[7:0], D1[7:0], D2[7:0] to DCLK	5	-	-	ns
DE setup time	T_{esu}	-	5	-	-	ns
DE hold time	T_{ehd}	-	5	-	-	ns
Output stable time	T_{sst}	10% to 90% target voltage. CL=90pF, R=10KΩ **(Cascade)**	-	-	6	μs
		Dual gate			3	

Table : TTL mode AC electrical characteristics

5.5.2 TTL mode data input format

- **Vertical timing**

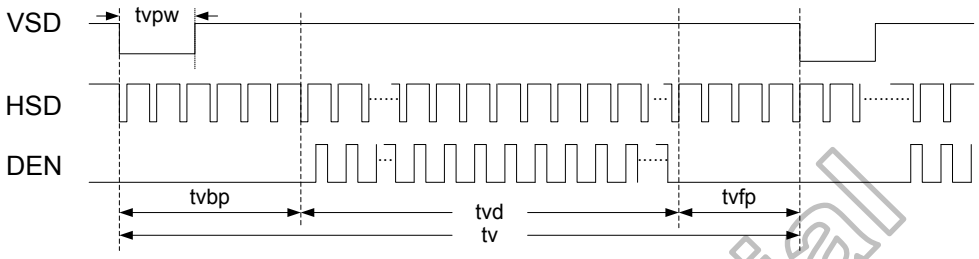


Figure: Vertical input timing diagram

- **Horizontal timing**

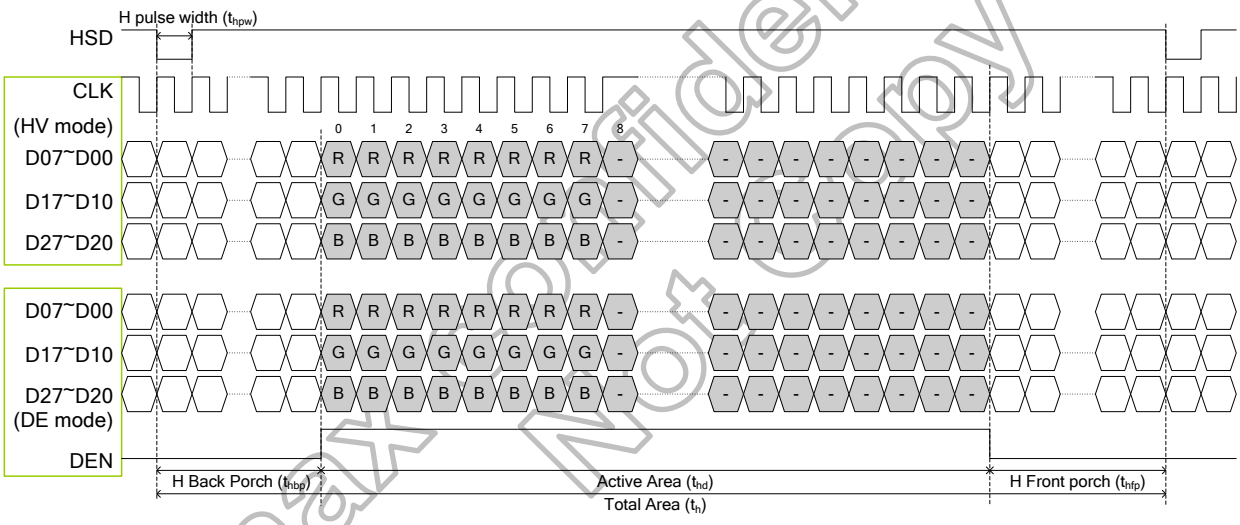


Figure: Horizontal input timing diagram

5.5.3 Input timing table

DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	40.8	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSD period	th	1114	1344	1400	DCLK
HSD blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		T_H
VSD period	tv	610	635	800	T_H
VSD blanking	tvbp+tvfp	10	35	200	T_H

Table: DE mode (1024x600)

HV mode

- **Horizontal timing**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	44.9	51.2	63	MHz
Horizontal display area	thd		1024		DCLK
HSD period	th	1200	1344	1400	DCLK
HSD pulse Width	thpw	1	-	140	DCLK
HSD back porch	thbp		160		DCLK
HSD front porch	thfp	16	160	216	DCLK

Table : HV mode horizontal timing (1024x600)

- **Vertical timing**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		T_H
VSD period	tv	624	635	750	T_H
VSD pulse width	tvpw	1	-	20	T_H
VSD back porch	tvbp		23		T_H
VSD front porch	tvfp	1	12	127	T_H

Table: HV mode vertical timing (1024x600)

5.6 Timing Diagram of Interface Signal

5.6.1 Input clock and data timing diagram

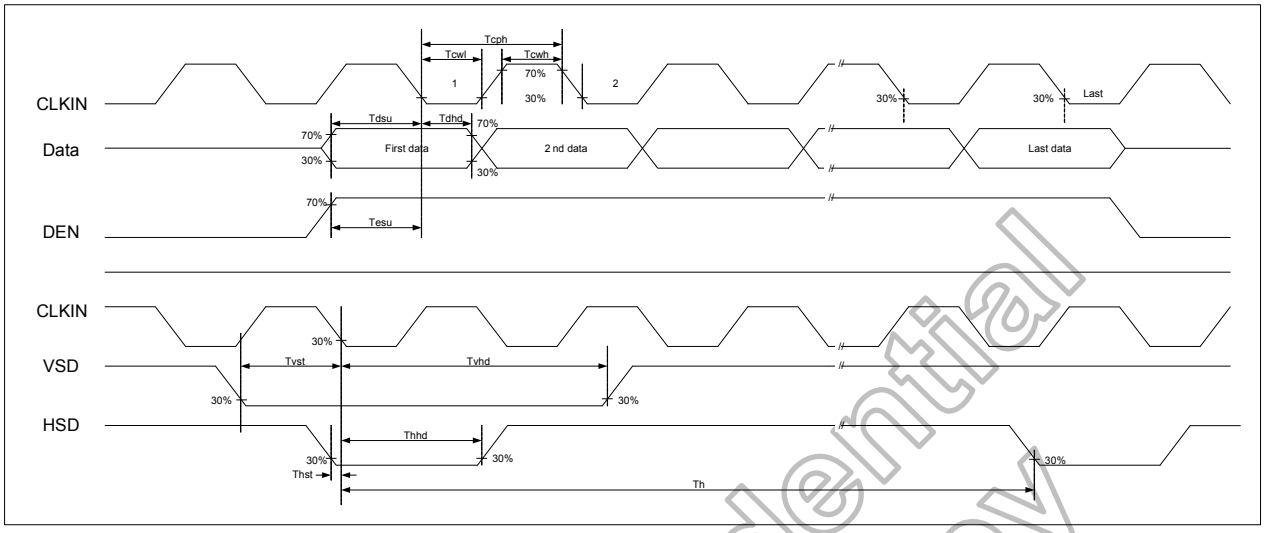


Figure: Input clock and data timing diagram

5.6.2 Source output timing diagram (Cascade)

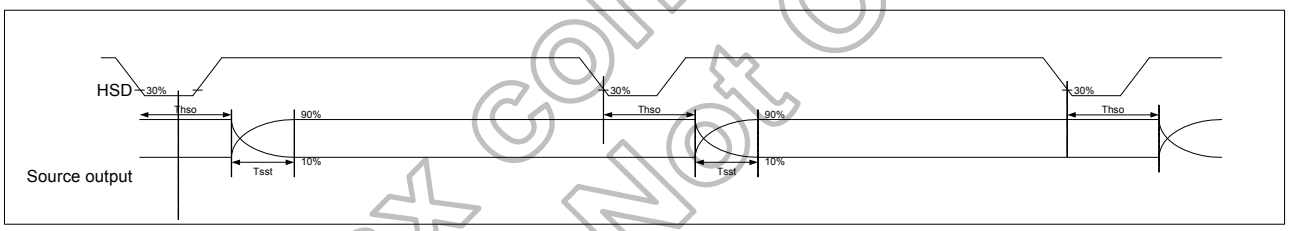


Figure 11.2: Source output timing diagram

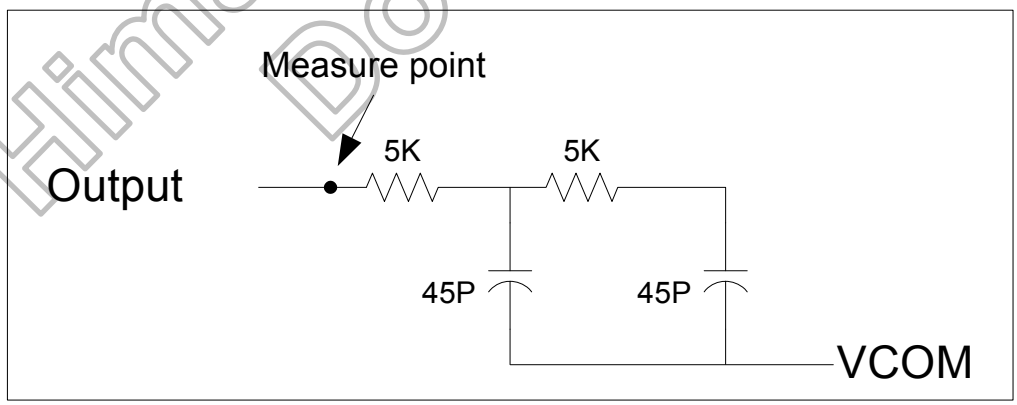


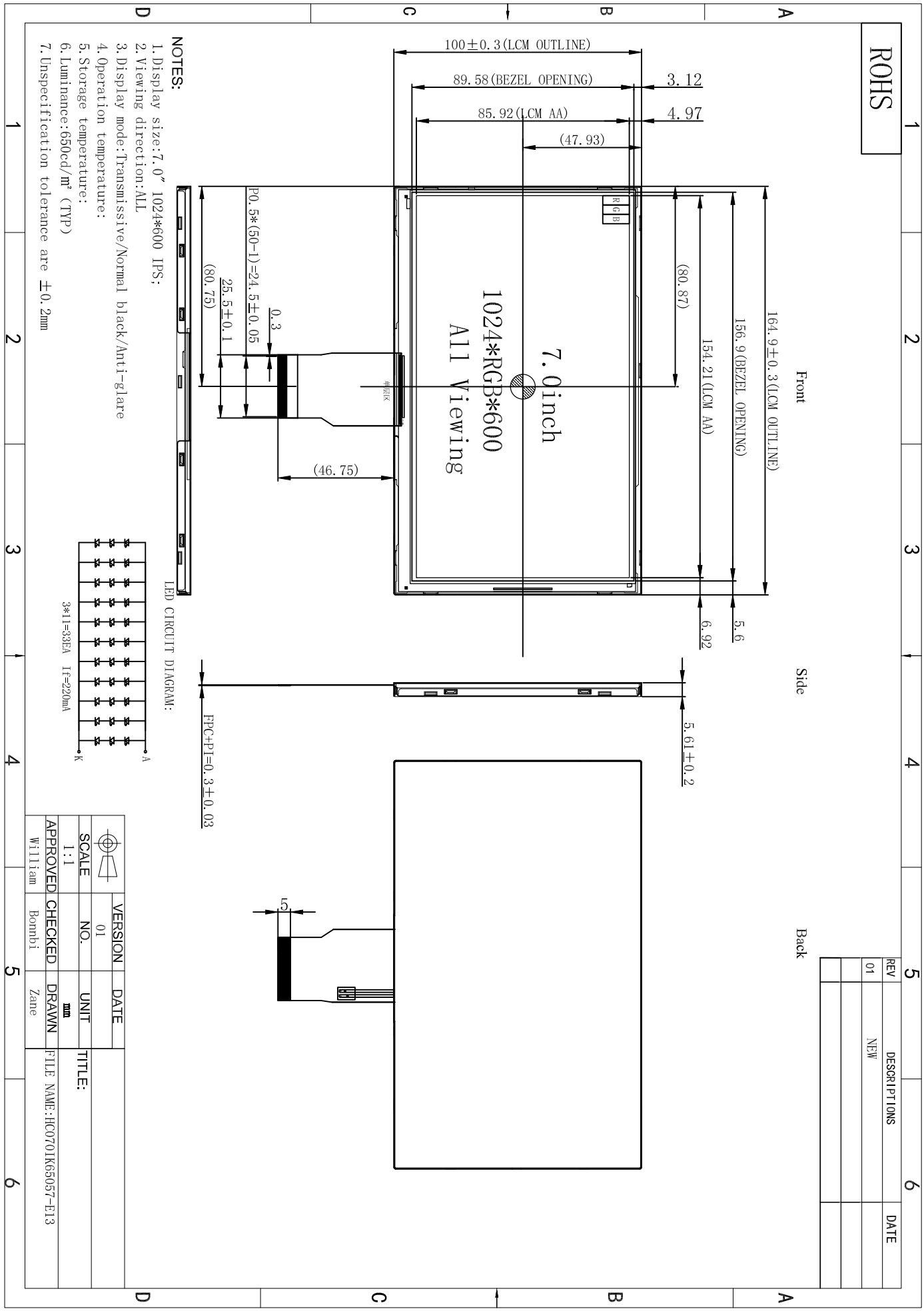
Figure: Output load condition

6.0 Reliability test items

Item	Test Conditions	Remark
High Temperature Storage	Ta = 80℃ 96hrs	Note 1，Note 4
Low Temperature Storage	Ta = -30℃ 96hrs	Note 1，Note 4
High Temperature Operation	Ts = 70℃ 96hrs	Note 2，Note 4
Low Temperature Operation	Ta = -20℃ 96hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH 96hrs	Note 4
Thermal Shock	-20℃/30 min ~ +70℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature.	Note 4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : ISTA-3A 1Hz~200Hz,Grms=0.53 Half hours for direction of Z.	
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

7.0 OUTLINE DIMENSION



8.0 General precaution

8.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

8.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HC does not warrant the module, if customers disassemble or modify the module.

8.3 Breakage of LCD Panel

8.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

8.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

8.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

8.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

8.4 Electric Shock

8.4.1. Disconnect power supply before handling LCD module.

8.4.2. Do not pull or fold the LED cable.

8.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

8.5 Absolute Maximum Ratings and Power Protection Circuit

8.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

8.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

8.5.3. It's recommended to employ protection circuit for power supply.

8.6 Operation

8.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

8.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

8.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

8.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

8.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

8.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

8.8 Static Electricity

8.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

8.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

8.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.